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Technical Briefs

ESD During Times of Change

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The electrostatic discharge (ESD) threat is a perennial issue dating back to the beginning of the semiconductor technology development [1]. No one is quite certain when it was first observed and recognized as a real threat to the electronics industry but it has not received clear focus until the late 1970s when the first ESD symposium was held. It was during this time that both control measures were implemented in areas where ICs are handled (ESD protected areas), and ESD protection structures were added to the IO circuitry. As industry experts have realized that charges on humans is a major source of damage the commonly known Human Body Model (HBM) test was developed. Similarly discharge from packaged ICs touching grounded metal surfaces led to the introduction of Charge Device Model (CDM). Applying these test models typical failures found during handling of semiconductors can be reproduced (Figure 1). They are distinctly different to extended fails when an electronic system is hit by a massive electrical overstress or ESD discharge (Figure 1). For many years it was believed that IC design protection to 2000 V HBM and 500 V CDM should be absolutely required for safe production and handling. However, this scenario started changing due to aggressive device scaling effects starting during the early 1980s and the demand for higher speed

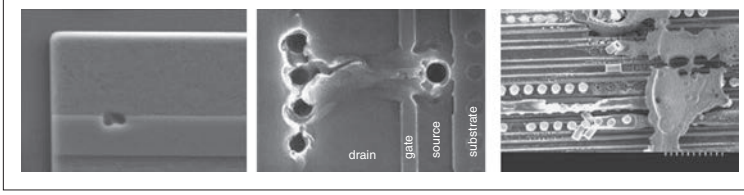

Fig. 1. IC damages due to ESD: CDM type (left), HBM type (middle), system level ESD (right).

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Your Comments Solicited

Your comments are most welcome. Please write directly to the Editor-in-Chief of the Newsletter at radhakrishnan@ieee.org

EDS-ETC Report from the AP/ED/MTT/COM/EMC Tomsk Chapter

Oleg Stukach, Vice Chair of Tomsk Chapter

The Chapter used a new approach for the utilization of EDS-ETC Snap Circuits Kits. This year for the first time the Chapter employed the "Open Door Days" of the Institute of Cybernetics of Tomsk Polytechnic University (TPU) for Snap Kit demonstrations among school children. Normally this event promotes training programs and curriculum description of the Institute for fresh students who intend to join the University in summer. Majority of the school children can apprehend information only in the game form. It is the result of relation to the engineering education. The Snap Circuits kits were used to demonstrate physical laws and simultaneously the practical applications, which was demonstrated this year with the full involvement of students. The children responded very positively by asking various questions related to electronics engineering during the session. Thus, these gadgets helped to provide more practical knowledge and to show the engineering subject is more interesting. Since the beginning of 2015 the Chapter has held three high-grade meetings of this nature, and plan to continue this type of program.

School children practicing utilizing the Elenco Snap Circuits© Kit

ED Calcutta Chapter EDS-ETC Program

The ED Calcutta Chapter with active support from the student members of the ED University of Calcutta Student Branch Chapter organized an EDS-ETC Program on March 31, 2015 at 'Brahmo Balika Shikshaloy.' A total number of 16 projects were carefully selected and demonstrated to the students with the help of the Elenco Snap Circuits® kits. The basic ideas of transistor, solar cell, digital logic gates were explained to the students by the EDS University of Calcutta Student Branch Chapter.

EDS-ETC program held at Brahmo Balika Shikshaloy